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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,475	03/26/2004	Tetsu Hasegawa	251144US2	8330
22850	7590	09/13/2006	EXAMINER	
C. IRVIN MCCLELLAND OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			RADOSEVICH, STEVEN D	
		ART UNIT	PAPER NUMBER	
			2138	

DATE MAILED: 09/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/809,475	HASEGAWA ET AL.
	Examiner	Art Unit
	Steven D. Radosevich	2138

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 25 July 2006.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-20 is/are pending in the application.
 4a) Of the above claim(s) 19 and 20 is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-18 is/are rejected.
 7) Claim(s) 3,9-11,13,15 and 17 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 26 March 2004 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>8/16/04</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Claims 1-20 are present for examination.

Priority

Acknowledgement is made that foreign priority is claimed for this application and as such the date (03/26/2003) is being used for this examination.

Information Disclosure Statement

Acknowledgement is made that an Information Disclosure Statement (IDS) was provided with the application and has been fully considered.

Drawings

The drawings are accepted since the examiner does not see at this time any errors wherein the drawings would need to be corrected or require an objection.

Election/Restrictions

Applicant's election without traverse of claims 1-18 in the reply filed on 07/25/2006 is acknowledged.

Claim Objections

Claim 3 is objected to because of the following informalities:

The word, "which" should be, inserted between "result signature" and "fails to" in line 3 on page 94 to make the claim read correctly.

Claim 9 is objected to because of the following informalities:

It is unclear to the examiner how there is a "second data compression units" in line 3 of the claim wherein there are no prior "first" compression units within the claim or claims that the claim is dependent on.

It is unclear to the examiner how there is a “second parallel to serial converter” in line 8 of the claim wherein there is no prior “first” parallel to serial converter within the claim or claims that the claim is dependent on.

Claim 10 is objected to because of the following informalities:

It is unclear to the examiner how there is a “second selector” in line 3 of the claim wherein there is no prior “first” selector within the claim or claims that the claim is dependent on.

It is unclear to the examiner how there is a “second data compression units” in line 5 of the claim wherein there are no prior “first” compression units within the claim or claims that the claim is dependent on

It is unclear to the examiner how there is a “second parallel to serial converter” in line 10 of the claim wherein there is no prior “first” parallel to serial converter within the claim or claims that the claim is dependent on.

Claim 11 is objected to because of the following informalities:

It is unclear to the examiner how there is a “second selector” in line 3 of the claim wherein there is no prior “first” selector within the claim or claims that the claim is dependent on.

Claim 13 is objected to because of the following informalities:

It is unclear to the examiner how there is a “second selector” in line 3 of the claim wherein there is no prior “first” selector within the claim or claims that the claim is dependent on.

Claim 14 is objected to because of the following informalities:

It is unclear to the examiner how there is are “second data compression units” in line 6 of the claim wherein there are no prior “first” compression units within the claim or claims that the claim is dependent on.

It is unclear to the examiner how there is a “second parallel to serial converter” in line 11 of the claim wherein there is no prior “first” parallel to serial converter within the claim or claims that the claim is dependent on.

Claim 15 is objected to because of the following informalities:

There should be a space placed within the word “configuredto” in line 7 on page 101 so that it reads “configured to.”

Claim 17 is objected to because of the following informalities:

There is not a “.” at the end of the limitation on page 102 line 3 of the claim which is required.

Appropriate correction is required for all objections.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 1-18, it is unclear to the examiner after reviewing the specification what the applicant is means by a “first order,” “second order,” “third order,” and “fourth

order" which is present throughout the claims. Applicant is respectfully requested to give further explanation to the unclear subject matter.

As per claims 1 and 6, it is unclear to the examiner after reviewing the specification what applicant intends within the claim wherein the test results are transferred to the scan chains in a first order when the test results were produced from the output data of the scan chains. It is the examiner's understanding that data or a test pattern is provided to the scan chains, which in turn execute the test and retrieve test results from a device under test (DUT), and outputs the results for analysis; nowhere do the test results of the test get inputted back into the scan chain(s). Appropriate correction or explanation as to transferring the test results to the scan chain in a first order is required to overcome this rejection.

Claim 7 recites the limitation "the block test results" in line 7 of the claim. There is insufficient antecedent basis for this limitation in the claim. Examiner notes that there is not prior reference to "block test results" or "blocks" in the claim or claims the claim is dependent on. Additionally it is unclear to the examiner if the "block compression unit" in the claim in lines 5-6 on page 96 is the same as the "test result compression unit" within claim 1, in line 8 on page 93, which claim 7, is dependent on. If these units are one in the same then the third limitation of claim 7 does not further limit the claimed subject matter of claim 1. For the purposes of this examination and further examinations they will be treated as being one in the same as such will all other additional compression units unless stated by the applicant to be otherwise.

Claim 12 recites the limitation "the divided blocks" in line 14 of the claim. There is insufficient antecedent basis for this limitation in the claim. Examiner notes that there is no prior reference to "divided blocks" or "blocks" within the claim or the claims that claim 12 is dependent on and that the "block test results" on line 12 of the claim are interpreted to be the results of the "failure block determination mode," title of a mode.

Claim 13 recites the limitation "the failure scan chain determination mode" in line 12 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim 16 recites the limitation "the block expected value comparison circuit" and "the corresponding expected values" in lines 1-4 of the claim. There is insufficient antecedent basis for this limitation in the claim. Examiner notes that there is not prior reference to any comparison circuit in the claim or claims the claim is dependent on.

Claims 2-18 are dependent on claim 1 and therefore also inherit the 35 U.S.C. 112, second paragraph issues of the claim and may not be further considered on their merits.

Claims 8-11 and 14-18 are dependent on claim 7 and therefore also inherit the 35 U.S.C. 112, second paragraph issues of the claim and may not be further considered on their merits.

Claims 13 is dependent on claim 12 and therefore also inherits the 35 U.S.C. 112, second paragraph issues of the claim and may not be further considered on its merits.

Double Patenting

1. Claims 1-3 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 4 of copending Application No.10426657 also known as US Publication 20030229886. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 4 of the copending application is more specific than claims 1-3 which indicates that claims 1-3 are anticipated by claim 4 of the copending application. Claim 4 of the copending application in addition to containing a test pattern generator (TGP), a compressor, a plurality of scan chains, a comparison circuit, and failure information output circuit which are all present in claims 1-3 of the instant application contains a first, second, third external terminals as described in detail within the copending application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

2. Claim 4 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 4, figures 5 and 16, and pages 1-3 of the specification of copending Application No. 10426657 also known as US Publication 20030229886. Although the conflicting claims are not identical, they are not patentably distinct from each other because although it is not explicitly written within the copending application that a parallel to serial converter is used to produce the single signal 110 (figure 16 and page 3 line 6 of the specification of copending application 10426657) one or ordinary skill in the art at the time the invention was made would recognize that a

parallel to serial conversion is done to convert the "parallel shift register sequence generator (STUMPS) system" (page 2 lines 2-3 of the specification of the copending application) test results supplied to the test result compressor 16 (figure 16 and page 3 lines 2-3 of the specification of the copending application) to produce the single signal 110 (serial signal) indicating a test analysis result (page 3 of the specification of copending application). Claim 4 of the copending application therefore contains in addition to everything as described above regarding claims 1-3, the data compression units within the compression unit (figure 5 of the copending application), and the parallel to serial converter.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

3. Claim 5 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 4 and figures 5, 9, and 16 of copending Application No. 10426657 also known as US Publication 20030229886. Although the conflicting claims are not identical, they are not patentably distinct from each other because figure 9 of the copending application shows that a selector (917) is connected to the output terminals of the result compressor (912) not the scan chains (913) and it would have been obvious to one having ordinary skill in the art at the time the invention was made to move the selector (917) to between the scan chains (913) and the compressor (912), since it has been held that rearranging parts of an invention involves only routine skill in the art, *IN re Japikse*, 86 USPQ 70. Claim 4 of the copending application therefore contains everything as described above regarding

claims 1-3, the data compression units within the compression unit (figure 5 of the copending application), and the parallel to serial converter (as described above in claim 4).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1,2, 6, and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Coteet at (US Patent 6671839 B1).

4. As per claim 1, Coteet teaches an integrated circuit comprising:

Scan chains implemented by registers disposed in a logic circuit, configured to shift in test patterns, to transfer the test patterns to the logic circuit, to receive test results of the logic circuit, and to shift out the test results (column 1 lines 14-18, column 3 lines 46-60 with figure 2, and column 4 lines 4-12 with figure 2);

A test pattern generation unit configured to transform the test patterns as scanning test patterns for feeding into the scan chains (column 1 lines 20-26, column 3 lines 46-60, and column 7 lines 10-19); and

A test result compression unit connected to the output stages of the scan chains, configured to compress the test results so as to generate the same number of compressed test result signatures as the number of the test results, and to transfer the resulting compressed test result signatures to the scan chains in a first order to allow one-to-one mapping (column 1 lines 20-26, column 3 lines 46-60 and column 4 lines 12-16).

5. As per claim 2, Coteet teaches the integrated circuit further comprising:

An expected value comparison circuit configured to compare the compressed test result signatures with a corresponding expected value in the first order, and detects a compressed test result signature which fails to match the corresponding expected value (column 4 lines 10-16, column 1 lines 20-25, and column 3 lines 50-54).

6. As per claim 6, Coteet teaches the integrated circuit wherein the test result compression unit comprises:

A mode changeover circuit connected to the output stages of the scan chains configured to receive the test results in parallel and output the test results in parallel in a self-test mode, to receive the test results in parallel in a failure analysis mode, and to transfer the test results to the scan chains in a first order

that allows one-to-one mapping (figure 2, column 1 lines 13-26, column 3 lines 45-55, and column 4 lines 10-16); and

A data compression unit connected to the mode changeover circuit configured to receive the test results in parallel in the self-test mode, to collectively compresses the test results into a single compressed test result signature, and to compresses the test results in the first order in the failure analysis mode (column 1 lines 20-26, column 3 lines 45-55, and column 4 lines 10-16).

7. As per claim 7, the integrated circuit wherein the test pattern generation unit divides the test pattern, generating scanning test patterns;

The scan chains shift in the scanning test patterns and simultaneously transfer the scanning test patterns to the logic circuit, receive the test results from the logic circuit, and shift out the block test results dividing the test results from respective last stages of block in the scan chains (column 7 lines 10-19); and

The integrated circuit further comprising a block compression unit configured to receive the block test results, to compress the test results so as to generate the same number of compressed test result signatures as the test results, and to transfer the resulting compressed block test result signatures to the blocks in a third order that allows one-to-one mapping (column 1 lines 20-25, column 3 lines 45-55, column 4 lines 10-15).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 3, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteet at. (US Patent 6671938 B1) as applied to claims 1-2 above, and further in view of Sager et al (US Patent 4342084).

8. As per claims 3, 12, and 13, Coteet teaches the integrated circuit as described above in detail, comprising: scan chains, a test pattern generator (TPG), a test result compression unit, and an expected value comparison unit. Taught by Coteet yet not described above in detail are counters within the integrated circuit, pattern and bit counters (figure 2 and columns 3-4 lines 65-2). Also taught in Coteet are changes in test mode and parallel processing (see figure 2).

Coteet does not specifically teach wherein the integrated circuit further comprising:

A failure scan chain determination circuit configured to count the order of a compressed test result signature fails to match the corresponding expected value during comparison in the first order, and determines a failure scan chain, which includes a failure detected in the scan chains.

However in an analogous art Sager teaches the need to replace or repair parts/components that have not past testing or that have resulted a circuit/device under test (DUT) to not pass testing, wherein the determination of passing or not passing testing is dependent upon the value or magnitude of errors detected and counted. The art is replete with such references that teach this, Sager is but one.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to modify Coteet's teachings so that a counter count errors detected such as taught by Sager so that the expected value comparison unit can expedite test execution and thus expedite the execution of repair or replacement of faulty scan chains since additional time does not need to be spent on analyzing further data from a scan chain when the magnitude of errors exceeds the value in which it does not pass the testing.

Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteet at. (US Patent 6671938 B1) as applied to claim 1 above.

9. As per claim 4, Coteet teaches the integrated circuit wherein the test result compression unit includes:

Data compression units connected to the respective output terminals of the scan chains, configured to receive the test results, and to transfer the compressed test result signatures, the number of the data compression units is the same as the number of the test results (column 3 lines 45-55 and column 4 lines 25-30)

Coteet does not specifically teach wherein the test result compression unit includes:

A parallel to serial converter connected to all of the data compression units, configured to receive the compressed test result signatures in parallel, and to serially transfer the compressed test result signatures in the first order.

However Coteet does disclose a space compactor used to reduce the number of inputs to the MISR (column 4 lines 25-30). It would have been obvious to one having ordinary skill in the art at the time the invention was made to increase this reducing of a number of inputs down to a single input since the examiner take official notice of the equivalence of the space compactor and a parallel to serial converter for their use in the reduction of connections required art and the selection of any of these know equivalents to reduce pins and complexity of system connections would be within the level of ordinary skill in the art.

Furthermore, Coteet teaches the space compactor used prior it input to data compression. It would have been obvious to one having ordinary skill in the art at the time the invention was made to reposition the space compactor is being used after data

compression, since it has been held that mere reversal of the essential working parts of a device involves only routine skill in the art.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to reverse the order of the compression unit and the recognized equivalent space compactor within Coteet, wherein the space compactor placed prior to the compression unit is limiting efficiency by restricting the flow of data to the compression unit which provides less data output. The less data output by the compression unit would thus reduce or eliminate any restriction of data flow by the space compactor if placed after data had been compressed.

10. As per claim 5, Coteet teaches the integrated circuit wherein the test result compression unit comprises:

A first selector connected to the output terminals of the scan chains, configured to select and transfer the test results in a second order (column 4 lines 25-30).

Coteet does not specifically teach wherein the result compression unit comprises:

A plurality of data compression units connected to the first selector configured to receive the test results, and to transfer the compressed test result signatures, the number of the data compression units being smaller than the number of the test results; and

A parallel to serial converter connected to the data compression unit configured to receive the compressed test result signatures in parallel, and to serially transfer the compressed test result signatures in the first order.

However Coteet teaches a data compression unit (column 3 lines 45-55 and column 1 lines 23-26). It would have been obvious to one of ordinary skill in the art at the time the invention was made to duplicate the data compression unit to perform parallel processing and thus reducing execution time, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art.

St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

Furthermore, the parallel to serial converter and its location after the data compression unit configured to receive the compressed test result signature in parallel, and to serially transfer the compressed test result signature in the first order has been covered in the preceding claim, as per claim 4 as described in detail above.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to duplicate the data compression unit and reverse the order of the multiple compression units and the recognized equivalent space compactor within Coteet, wherein the space compactor placed prior to the compression unit is limiting efficiency by restricting the flow of data to the compression unit which provides less data output. The less data output by the compression unit would thus reduce or eliminate any restriction of data flow by the space compactor if placed after data had been compressed.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Coteet at. (US Patent 6671938 B1) as applied to claims 1 and 7 above, and further in view of Sager et al (US Patent 4342084).

11. As per claim 8, Coteet teaches the integrated circuit further comprising:

A block expected value comparison circuit configured to compare the compressed block test result signature with the corresponding expected value in a third order, and to detect a compressed block test result signature that fails to match the corresponding expected value (column 3 lines 45-55, column 1 lines 25-35, and column 4 lines 10-16).

Coteet does not specifically teach wherein the integrated circuit further comprises:

A failure block determination circuit configured to count the order of the compressed block test result signature that fails to match the corresponding expected value in the third order, and to identify a failure block having a failure detected in the blocks.

However in an analogous art Sager teaches the need to replace or repair parts/components that have not past testing or that have resulted a circuit/device under test (DUT) to not pass testing, wherein the determination of passing or not passing testing is dependent upon the value or magnitude of errors detected and counted. The art is replete with such references that teach this, Sager is but one.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to modify Coteet's teachings so that a counter count errors

detected such as taught by Sager so that the expected value comparison unit can expedite test execution and thus expedite the execution of repair or replacement of faulty scan chains since additional time does not need to be spent on analyzing further data from a scan chain when the magnitude of errors exceeds the value in which it does not pass the testing.

Claims 9, 10, 11, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteet at. (US Patent 6671938 B1) as applied to claims 1 and 7 above.

12. As per claims 9, 10, and 11, Coteet teaches the integrate circuit as described above in detail as per claims 1 and 7.

Coteet does not specifically teacher wherein the block compression unit comprises:

Second data compression units, connected to the output terminals of the blocks, configured to receive the block test results, and to transfer compressed block test result signatures, the number of the second data compression units is the same as the number of the block test results, and

A second parallel to serial converter configured to receive in parallel the compressed block test result signature from the second data compression units, which are connected to the divided blocks in one of the scan chains, and to serially transfer the compressed block test result signatures in the third order.

However Coteet does teach of a compression unit and an art recognized equivalent to a parallel to serial converter, as described above as per claim 4. It would

have been obvious to one having ordinary skill in the art at the time the invention was made to duplicate these components within the integrated circuit, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to duplicate these essential components within the intergraded circuit as taught by Coteet since it would implement parallel processing of data which as is well know would decrease the processing time required by the integrated circuit to execute or process data.

13. As per claim 14, Coteet teaches the integrate circuit wherein the block compression unit comprises:

An exclusive-OR calculation unit configured to transfer an exclusive-ORed value of the block test results, which are delivered from the scan chains including a failure scan chain (column 4 lines 18-21). Examiner notes that a LFSR is well known to have logic gates within used to either help expand or compress data. Coteet does not specifically teacher wherein the integrated circuit wherein the block compression unit comprises:

Second data compression units connected to the exclusive-OR calculation unit, configured to receive the exclusive-ORed value, and to transfer the compressed block result signatures, the number of the second data compression units is smaller that then number of the block test results; and

A second parallel to serial converter configured to receive in parallel the compressed block test result signatures from the second data compression unit connected to the divided blocks in one of the scan chains and to serially transfer the compressed block test result signatures in the third order.

However Coteet does teach of a compression unit and an art recognized equivalent to a parallel to serial converter, as described above as per claim 4. It would have been obvious to one having ordinary skill in the art at the time the invention was made to duplicate these components within the integrated circuit, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to duplicate these essential components within the intergraded circuit as taught by Coteet since it would implement parallel processing of data which as is well know would decrease the processing time required by the integrated circuit to execute or process data.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- i. Beffa (US Patent 6347386 B1) discloses the need to repair identified failing components or circuitry that do not or result in a devices failure to pass testing.

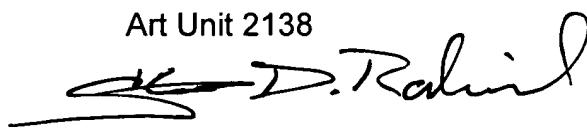
- ii. Kim (US Patent 5574733) discloses a linear feedback shift register (LFSR) and the use of a logic gate (XOR) within
- iii. Gupta (US Patent 6609222) discloses low power testing by selecting a finite number of locations within the being tested circuitry to be tested.
- iv. Forlenza (US patent 5930270) discloses and XOR used in conjunction with the output of a device that had been tested along with multiple input shift registers (MISR).
- v. Other references included/attached within the action within the 892 are directed to compression of test results as is well known to those of ordinary skill in the art at the time the invention was made, different modes within testing, bit-by-bit checking thus one-to-one mapping.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decay can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven D. Radosevich
Examiner
Art Unit 2138



JOSEPH TORRES
PRIMARY EXAMINER

